

## CLAIMS

- 1 1. Bridge apparatus for connecting a first multimaster bus I<sup>2</sup>C environment to a  
2 second multimaster bus I<sup>2</sup>C environment, comprising  
3 an address bitmap having a value associated with each possible I<sup>2</sup>C  
4 address;  
5 a port-A interface that receives address signals and data signals from the  
6 first multimaster and transmits data signals to the first multimaster bus;  
7 a port-B interface that transmits address signals and data signals to the  
8 second multimaster bus and received data signals from the second multimaster  
9 bus; and  
10 a controller that selectively passes an address and data received on the  
11 port-A interface from the first multimaster bus to the port-B interface for  
12 transmission on the second multimaster bus depending on the address bitmap  
13 value associated with the address.
- 1 2. The bridge apparatus of claim 1 wherein the controller comprises a command  
2 interpreter that receives commands at the port-A interface from the first  
3 multimaster bus and controls the operation of the bridge apparatus in response  
4 to received commands.
- 1 3. The bridge apparatus of claim 2 wherein a tunnel command received by the  
2 bridge apparatus includes a tunnel address and the controller passes the tunnel  
3 address to the port-B interface for transmission on the second multimaster bus.
- 1 4. The bridge apparatus of claim 2 further comprising a plurality of registers, each  
2 holding a value that control the operation of the bridge apparatus and wherein  
3 the command interpreter receives commands at the port-A interface from the first

- 4 multimaster bus and places a value in at least one of the registers in response  
5 thereto.
- 1 5. The bridge apparatus of claim 4 wherein a first register holds a bridge ID value  
2 and each command contains a bridge ID value and wherein the command  
3 interpreter comprises a mechanism which responds to a command when the  
4 bridge ID value therein equals the bridge ID in the first register.
- 1 6. The bridge apparatus of claim 5 wherein a second register defines a range of  
2 bridge IDs and wherein the command interpreter comprises another mechanism  
3 that transmits a received command on the second multimaster bus when the  
4 bridge ID in the received command is in the range of bridge IDs.
- 1 7. The bridge apparatus of claim 1 wherein the controller is a programmed  
2 microcontroller.
- 1 8. The bridge apparatus of claim 7 wherein the microcontroller comprises a RAM  
2 memory wherein the address bitmap is located.
- 1 9. The bridge apparatus of claim 7 wherein the microcontroller is connected to the  
2 port-A interface by a clock and data line and the microcontroller detects a START  
3 signal by generating an interrupt based on a signal on the data line.
- 1 10. Bi-directional bridge apparatus for connecting a first multimaster bus I<sup>2</sup>C  
2 environment and a second multimaster bus I<sup>2</sup>C environment, comprising  
3 a first unidirectional bridge device having, a first address bitmap having a  
4 value associated with each possible I<sup>2</sup>C address, a first port-A interface that  
5 receives address and data signals from the first multimaster bus, a first port-B

6 interface that transmits address and data signals to the second multimaster bus;  
7 and a first controller that selectively passes an address and data received on the  
8 port-A interface from the first multimaster bus to the port-B interface for  
9 transmission on the second multimaster bus depending on the first address  
10 bitmap value associated with the address and

11 a second unidirectional bridge device having, a second address bitmap  
12 having a value associated with each possible I<sup>2</sup>C address, a second port-A  
13 interface that receives address and data signals from the second multimaster  
14 bus, a second port-B interface that transmits address and data signals to the first  
15 multimaster bus; and a second controller that selectively passes an address and  
16 data received on the port-A interface from the second multimaster bus to the  
17 port-B interface for transmission on the first multimaster bus depending on the  
18 second address bitmap value associated with the address.

1 11. The bi-directional bridge apparatus of claim 10 wherein both the first and second  
2 unidirectional bridge devices have a mechanism for designating whether a  
3 unidirectional bridge device is one of an upstream bridge and a downstream  
4 bridge.

1 12. The bi-directional bridge apparatus of claim 10 further comprising a deadlock  
2 mechanism for choosing one of the unidirectional bridge devices when both  
3 unidirectional bridge devices simultaneously begin a transaction.

1 13. The bi-directional bridge apparatus of claim 10 wherein the first unidirectional  
2 bridge device further comprises a plurality of registers, each holding a value that  
3 control the operation of the first unidirectional bridge device and wherein the first  
4 controller comprises a first command interpreter that receives commands at the  
5 port-A interface from the first multimaster bus and places a value in at least one  
6 of the registers in response thereto.

- 1 14. The bi-directional bridge apparatus of claim 13 wherein each of the commands  
2 contains a bridge ID and at least one of the registers defines a range of bridge  
3 IDs and wherein the first command interpreter comprises a mechanism that  
4 transmits a received command on the second multimaster bus when the bridge  
5 ID in the received command is in the range of bridge IDs.
- 1 15. The bi-directional bridge apparatus of claim 10 wherein the second unidirectional  
2 bridge device further comprises a plurality of registers, each holding a value that  
3 control the operation of the second unidirectional bridge device and wherein the  
4 second controller comprises a second command interpreter that receives  
5 commands at the port-A interface from the second multimaster bus and places a  
6 value in at least one of the registers in response thereto.
- 1 16. The bi-directional bridge apparatus of claim 15 wherein each of the commands  
2 contains a bridge ID and at least one of the registers defines a range of bridge  
3 IDs and wherein the second command interpreter comprises a mechanism that  
4 transmits a received command on the first multimaster bus when the bridge ID in  
5 the received command is outside the range of bridge IDs.
- 1 17. The bi-directional bridge apparatus of claim 15 wherein a register in the first  
2 unidirectional bridge device holds a first bridge ID value and a register in the  
3 second unidirectional bridge device holds a second bridge value different from  
4 the first bridge ID value.
- 1 18. The bi-directional bridge apparatus of claim 13 wherein each command contains  
2 a bridge ID value and wherein the first command interpreter comprises a  
3 mechanism which responds to a command when the bridge ID value therein  
4 equals the bridge ID in the first register.

- 1 19. The bi-directional bridge apparatus of claim 17 wherein each command contains  
2 a bridge ID value and wherein the second command interpreter comprises a  
3 mechanism which responds to a command when the bridge ID value therein  
4 equals the bridge ID in the first register.
- 1 20. A method for connecting a first multimaster bus I<sup>2</sup>C environment to a second  
2 multimaster bus I<sup>2</sup>C environment, comprising  
3 (a) connecting the first multimaster bus to the second multimaster bus with a  
4 bridge having an address bitmap having a value associated with each  
5 possible I<sup>2</sup>C address, a port-A interface that receives address signals and  
6 data signals from the first multimaster and transmits data signals to the  
7 first multimaster bus and a port-B interface that transmits address signals  
8 and data signals to the second multimaster bus and received data signals  
9 from the second multimaster bus; and  
10 (b) selectively passing an address and data received on the port-A interface  
11 from the first multimaster bus to the port-B interface for transmission on  
12 the second multimaster bus depending on the address bitmap value  
13 associated with the address.
- 1 21. The method of claim 20 wherein step (b) comprises receiving commands at the  
2 port-A interface from the first multimaster bus and controlling the operation of the  
3 bridge apparatus in response to received commands.
- 1 22. The method of claim 21 wherein a tunnel command received by the bridge  
2 apparatus includes a tunnel address and wherein step (b) further comprises  
3 passing the tunnel address to the port-B interface for transmission on the second  
4 multimaster bus.

- 1 23. The method of claim 21 wherein the bridge further comprises a plurality of  
2 registers, each holding a value that control the operation of the bridge apparatus  
3 and wherein step (b) comprises receiving commands at the port-A interface from  
4 the first multimaster bus and places a value in at least one of the registers in  
5 response thereto.
- 1 24. The method of claim 23 wherein a first register holds a bridge ID value and each  
2 command contains a bridge ID value and wherein step (b) comprises responding  
3 to a command when the bridge ID value therein equals the bridge ID in the first  
4 register.
- 1 25. The method of claim 24 wherein a second register defines a range of bridge IDs  
2 and step (b) comprises transmitting a received command on the second  
3 multimaster bus when the bridge ID in the received command is in the range of  
4 bridge IDs.
- 1 26. The method of claim 20 wherein the bridge comprises a programmed  
2 microcontroller that performs step (b).
- 1 27. The method of claim 26 wherein the microcontroller comprises a RAM memory  
2 wherein the address bitmap is located.
- 1 28. The method of claim 26 wherein the microcontroller is connected to the port-A  
2 interface by a clock and data line and the microcontroller detects a START signal  
3 by generating an interrupt based on a signal on the data line.
- 1 29. A method for connecting a first multimaster bus I<sup>2</sup>C environment and a second  
2 multimaster bus I<sup>2</sup>C environment, comprising

- 3 (a) connecting the first multimaster bus to the second multimaster bus with a  
4 first unidirectional bridge device having, a first address bitmap having a  
5 value associated with each possible I<sup>2</sup>C address, a first port-A interface  
6 that receives address and data signals from the first multimaster bus, a  
7 first port-B interface that transmits address and data signals to the second  
8 multimaster bus;
- 9 (b) selectively passing an address and data received on the port-A interface  
10 from the first multimaster bus to the port-B interface for transmission on  
11 the second multimaster bus depending on the first address bitmap value  
12 associated with the address;
- 13 (c) connecting the second multimaster bus to the first multimaster bus with a  
14 second unidirectional bridge device having, a second address bitmap  
15 having a value associated with each possible I<sup>2</sup>C address, a second port-  
16 A interface that receives address and data signals from the second  
17 multimaster bus, a second port-B interface that transmits address and  
18 data signals to the first multimaster bus; and
- 19 (d) selectively passing an address and data received on the port-A interface  
20 from the second multimaster bus to the port-B interface for transmission  
21 on the first multimaster bus depending on the second address bitmap  
22 value associated with the address.

1 30. The method of claim 29 wherein both the first and second unidirectional bridge  
2 devices have a mechanism for designating whether a unidirectional bridge device  
3 is one of an upstream bridge and a downstream bridge.

1 31. The method of claim 29 further comprising a deadlock mechanism for choosing  
2 one of the unidirectional bridge devices when both unidirectional bridge devices  
3 simultaneously begin a transaction.

- 1 32. The method of claim 29 wherein the first unidirectional bridge device further  
2 comprises a plurality of registers, each holding a value that control the operation  
3 of the first unidirectional bridge device and wherein step (b) comprises receiving  
4 commands at the port-A interface from the first multimaster bus and placing a  
5 value in at least one of the registers in response thereto.
- 1 33. The method of claim 32 wherein each of the commands contains a bridge ID and  
2 at least one of the registers defines a range of bridge IDs and wherein step (b)  
3 comprises transmitting a received command on the second multimaster bus  
4 when the bridge ID in the received command is in the range of bridge IDs.
- 1 34. The method of claim 29 wherein the second unidirectional bridge device further  
2 comprises a plurality of registers, each holding a value that control the operation  
3 of the second unidirectional bridge device and wherein step (d) comprises  
4 receiving commands at the port-A interface from the second multimaster bus and  
5 placing a value in at least one of the registers in response thereto.
- 1 35. The method of claim 34 wherein each of the commands contains a bridge ID and  
2 at least one of the registers defines a range of bridge IDs and wherein step (d)  
3 comprises transmitting a received command on the first multimaster bus when  
4 the bridge ID in the received command is outside the range of bridge IDs.
- 1 36. The method of claim 34 wherein a register in the first unidirectional bridge device  
2 holds a first bridge ID value and a register in the second unidirectional bridge  
3 device holds a second bridge value different from the first bridge ID value.



1 37. The method of claim 36 wherein each command contains a bridge ID value and  
2 wherein step (b) comprises responding to a command when the bridge ID value  
3 therein equals the bridge ID in the first register.

1 38. The method of claim 37 wherein each command contains a bridge ID value and  
2 wherein step (d) comprises responding to a command when the bridge ID value  
3 therein equals the bridge ID in the first register.